A Multi-Spatial Multi-Temporal Format Scanned Camera,

A versatile HDTV camera that can be used in 2-speed Super Slo Motion too

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Abstract

This paper describes the basics underpinning the design of the New SloMo HDTV camera. One of its remarkable features is the ability to use it in all the standard HDTV broadcast modes while also having the ability to operate in the 2X speed domain. This was clearly demonstrated at the recent European Soccer games in Portugal and shortly after at Summer Olympics in Athens Greece, where almost 20 of the newly developed camera systems were successfully used and integrated into daily broadcasts. The focus of this paper will be on the image sensor design and capabilities. Discussed will be the specially developed imager driving techniques that have pushed the technological boundaries of the sensor and associated hardware. It will be shown that the same technique can also be migrated into the VIPER FilmStream Digital Cinematography camera for 1080p60 imaging.

1.0 The Multi-Spatial and Multi-Temporal Format Scanned Imager

The basic specification of the HD-DPM imager as defined by Thomson and implemented by DALSA was based on the numerous scanning formats available nowadays and the need for one imager to handle all of these [1]. The basic photosensitive element has a dimension of 5umx1.25um (HxV). Through the use of 4320 vertical photosensitive elements in each of the 1920 columns one can generate all the Table 1 scanning formats in 16:9, unless otherwise stated. Starting from 1440p as the highest possible scanning format it can go down through 1080p, 720p, 1080i, 480p, 576i stopping at 480i. Other scanning formats are possible but are not yet within standardization and hence not tabulated. In the first column the number of vertical photogates is given that are added together to arrive at the scanning formats shown in the second column. The third column shows a mathematical notation for the scanning formats, which are, know as log-prime notation [2]. Here the scanning numbers are decomposed into primes and the 'log' of each prime taken.

#PHOTOGATES ADDED	SCANNING FORMAT	LOG PRIME NOTATION base [2,3,5,7,9,11]
3	1440p of which 1080p is derived with 2.37:1 aspect ratio	
4	1080p	[3,3,1,0,0,0]LP6
6	720p	[4,2,1,0,0,0]LP6
8	1080i	[2,3,1,0,0,0]LP6
9	480p	[5,1,1,0,0,0]LP6
15	576i or PAL	[5,2,0,0,0,0]LP6
18	480i or NTSC	[4,1,1,0,0,0]LP6

Table 1: The scanning formats available in the HDTV-DPM imager.

A remarkable property of this imager is the fact that the image diagonal is 11mm (2/3") for ALL 16:9 scanning formats in Table 1.
Anti-aliasing properties are scaled automatically with scanning format due to the special properties DPM imagers have [1,3,4,5].

It is clear, from Table 1, that both HDTV and SDTV standards are within reach.
The main reason for being able to generate these was of course the elegant geometric relationship between scanning formats and a sweet spot for the number of photosensitive element in every of the 1920 columns. This observation shows clearly in the log-prime notation. An extension to the geometric numbering can be found in many of the broadcast standards [6]

The LDK6000 and LDK6200 HDTV camera uses a subset of Table 1:The 720p and 1080i scanning formats. In VIPER the 1080p in 16:9 and 1440p to obtain 1080p in 2.37:1 aspect ratio are also available.

Multi-Temporal Scanned
Next to the spatial scanning there is also the question of the number of images-per-second known as temporal scanning. Already known are 1080p24, 1080p25, 1080p30, 1080i50, 1080i60, 720p24, 720p25, 720p30, 720p50 and 720p60. With the 2-speed HDTV camera this is extended into 1080i100 and 1080i120, for the first models.
Even when the camera is used in interlaced mode, the imager always scannes in progressive mode, Fig1. So let's assume the camera is used in 1080i60 mode. Which effectively means that 30 full frames per second are generated which are made up of an odd- and an even field. The fields are generated at 60 Fields per second. Then in the image-array 60 full frames per second are generated, Fig 1a, which are transported during the vertical blanking into the storage-array. Here the charge-image is stored still as a progressive image and is refreshed 60 times a second. Finally when it is read out, depending on the mode the camera is in, progressive or interlaced, the final image, or actual TV-line, is generated in the horizontal shift register. The horizontal shift register is, for reasons, which will become apparent shortly, split in two. A field of an interlaced image consists of 540 lines. In the case of the 1-speed and 2-speed camera they are generated from a 1080p image through addition of two consecutive lines during the horizontal blanking. Two lines from the 1080 progressive charge image are transported into the horizontal registers and added to obtain one line of the 540 needed to make one field, of the 1080 interlaced image, line 1+2 ,line 3+4, …. In the vertical blanking the 1080p charge image in the storage array is refreshed with a new one from the image array. After which the interlacing between the odd and even fields is accomplished through offsetting for the other field e.g. adding line 2+3, line 4+5 etc. Reading only odd lines for the odd field and even lines for the even field will lead to a violation of Nyquist sample and reconstruction law with a flickering aliasing as a result. Adding two lines together, though, reduces aliasing and enhances sensitivity at the same time [1,3,5,7]
Hence for the standard HDTV camera the scanning rate, of the image- and storage-array of the imager, ranges from 24p up to 60p independent of 1080i/p. It's only at readout time that the final format is derived. The reason for not wanting to generate the 1080i60 from the 1080p60 image in the digital domain has, amongst others, to deal with noise.

Recently the LDK6000 camera operation has been extended with a 2-speed functionality. Now the image-array is capturing a charge-image in progressive fashion

120 times per second, Fig 1b. That charge-image is refreshed in the storage-array also in progressive mode and then gives a 120 times per second frame rate. It's in the horizontal registers that the charge-packets are added to generate 1080i120 from a 1080p120 image. Or 1080i100 from 1080p100 for that matter depending on the TV system.

1080P60 versus 1080i120

What is still puzzling is the discussion in the broadcast industry about 1080p60 without even mentioning 1080i120. The discussion is focused on 1080p60 even though present state of the art HDTV studios cannot handle the doubled data rate.
Commercially it is more interesting for both manufacturer and customer to consider 1080i120 since that's where the market is. We have already sold almost 30 High-speed HDTV cameras. For super slo-motion the signal is fed through EVS-equipment for recording and replay as an intermediate between studio environment and camera system. In 1-speed usage integrates directly into the studio.
Technically, the application of our HD-DPM imagers to both 1080i120 and 1080p60 are equivalent from a horizontal clock speed point of view. However, fast vertical transport is a completely different problem. The vertical blanking in 1080i is 22.5TVL but in 1080p its 45TVL, twice as long. So, for imagers suffering from a vertical timing deficiency it will be possible to generate 60p, but not 120i. A remarkable asymmetry is encountered now: "Any camera scanning in 1080i120 can scan in 1080p60 but not every camera scanning in 1080p60 can scan in 1080i120".

Adding signals in the charge domain …..noiseless

When adding two voltage sources together one can double the signal and gain 6dB. Assuming uncorrelated noise sources the noise power doubles and hence the noise-voltage increases with only 3dB. The net result is a gain of 3dB in signal-to-noise.
The same holds for adding the signals in the digital domain, the improvement in SN is 3dB.
There is one exception to the rule and that is adding signals in the charge domain. In the case of a CCD imager one can add the charges of two pixels together without increasing the noise in black. The reason being the signal flow: First (signal)charge is generated in the pixel and after transport through the horizontal shift registers is goes through the on-chip amplifier where noise is added. Adding the charge-packets is done before the noise generating on-chip amplifier. Hence the improvement in SN of 6dB gained, when signals are added in the charge domain. This is the main reason for not wanting to use a 1080p60 image to generate a 1080i60 image in the digital domain. One would loose the additional 3dB improvement in SN. Hence the reason for wanting to derive a lower scanned format at the imager in the charge domain where signals can be added without impacting the noise.

2.0 The 2-speed HDTV camera

Already many years ago a 3-speed camera for SDTV was developed for the World Cup Soccer games in France [8]. A similar scenario was unfolding for the European Soccer Cup in Portugal and then the 2004 Summer Olympics in Athens Greece shortly after. It had to be a HDTV system camera with a focus on high speed 1080i operation. Moreover it had to have a dual HD-SDI connection at the base station to integrate easily between normal and 2-speed operation (to the EVS recorder). In contrast with prior slo-motion

cameras this HDTV camera system is designed to be used in normal HDTV mode (1-speed mode) and in 2-speed mode.

From an operational point of view a 2-speed camera has an advantage over a 3-speed camera because 2-speed does not have problems with artificial lighting. E.g. given the European system with its 50Hz, then especially artificial lighting has a heavily modulated 100Hz light intensity. A 2x speed camera running at 1080i100 will match that type of illumination. A 3-speed camera (150Hz) will always be out of phase and needs an elaborate compensation system.

The performance of a camera starts with its imager. The basic operation of the 2-speed HDTV camera was granted through the choice of imager architecture. Already in an early stage the decision was taken to equip the imager with two horizontal shift registers instead of the classical 1. It reduces the clock frequency specification for the horizontal shift registers by a factor of 2 and adds some benefits in signal-to-noise while easing the burden on driving electronics.

E.g. In 1x speed mode the pixel clocks had to be 2x37.125 MHz instead of 74.25 MHz and in 2-speed mode 2x74.25 MHz instead of 148.5 MHz was needed.

The imager basics was set in an early stage and based on tungsten technology [9]. This same technology had been used for the SDTV DPM imager [3,4,5] and the first HDTV imager according the Eureka standard [10]. The technique has evolved to a level high enough to sustain these high clock frequencies, bandwidths and a basic light-sensing element of 5umx1.25um (HxV). Of the latter 4320 are used in every of the 1920 columns.

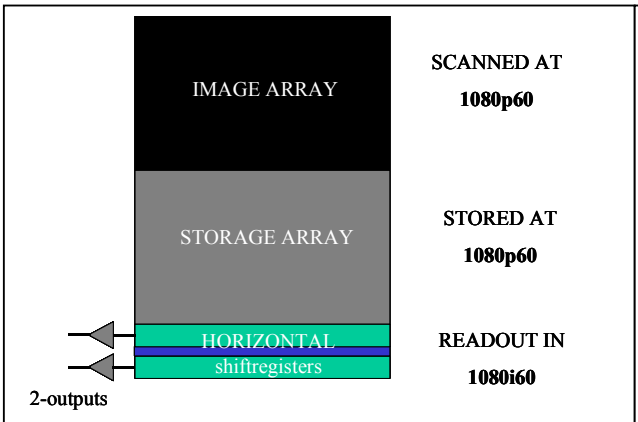

Fig 1a. : *LDK6200 in 1-speed mode; Shown is the scanning of the imager in 1080i60* mode

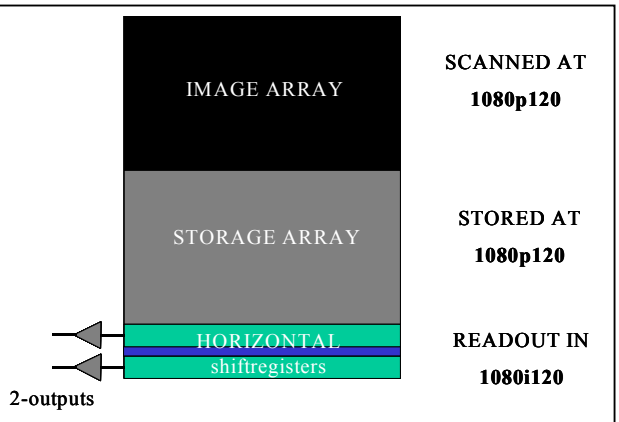

Fig 1b. : *LDK6200 in 2-speed mode; Shown is the scanning of the imager in 1080i120* mode

Timing aspects

The fast vertical transport is done in 4-phase fashion both for storage and image-array [1]. (For a recap on CCD imager operation see [11])

The driving phases of the storage-array are called B1, B2, B3 and B4 and are connected in a periodical manner. The 12-phases of the image are numbered A1, A2 …A12 to enable all the scanning formats, ref Table 1. Even though the horizontal register has a 4-phase driving mechanism, numbered C1…C4. It is used in quasi 2-phase mode during readout of the horizontal shift register to reduce the demand on the driving electronics. In quasi 2-phase mode only the clock (applied to C1 and C2) and the inverted clock

(applied to C3 and C4) are applied. The generation of the clock and its inverse is typically something that is much easier to accomplish than generating the clocks needed for a 4-phase transport where a duty cycle of 5/8 is needed and every phase is shifted over 1/4 of the master clock timing. The latter in 2-speed operation equals about 3.3ns. Designing the 2-speed HDTV camera needed a careful examination of the following timing aspects
-The **fast vertical transport** of the charge image in to the storage-array during, part of, the vertical blanking. Normally the transport frequency is 4.64 MHz and in 2-speed its 9.28 MHz.
-The **transport and redistribution** of the charge from the storage-array into the two horizontal shift registers during the horizontal blanking which is a relatively slow process.
-Reading the **horizontal registers** during the active line time at high speed, 37.125 MHz in normal operation and 74.25 MHz in 2-speed, to be combined into a pixel stream of 74.25 Mpps and 148.5 Mpps respectively in the processing afterwards.
Many of the problems to be tackled are due to the fact that in a 2-speed HDTV camera all the timing intervals are half those of a 1-speed HDTV camera. In the short time needed for the development of the 2-speed camera an answer was found in an early stage for the question of whether the imager could do 2x speed without having to build the application itself. It was decided to apply transmission line theory to the clock distribution in the imager to get an idea where the basic limitations would be in.

3.0 An analytical approach for the imager internal clock distribution

The horizontal transport register can be regarded as a huge number (thousands) of small resistor and capacitor values, Fig 2. The response of such a circuit can be approximated with a set of coupled differential equations. The operation of a CCD transport register is based on silicon overlaid with gates. They form the capacitances. The series resistance represents the interconnection to the gates.

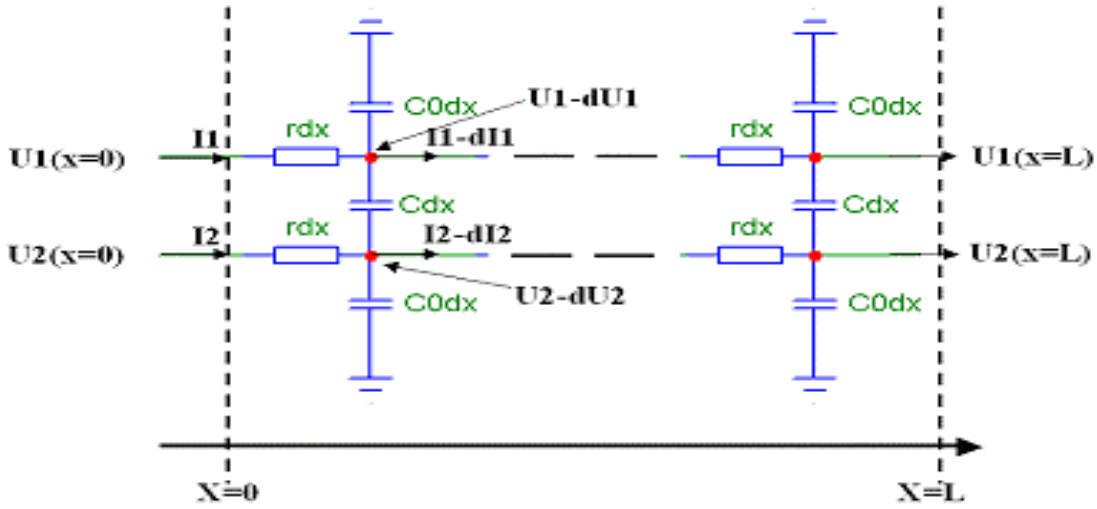

Fig 2: *The electrical replacement diagram of the horizontal shift registers used in quasi 2-phase driving mode. The length of the transmission line is* ***L*** *and is open at the end.* ***C0*** *is the capacitance per unit length to the ground and* ***C*** *is the coupling capacitance per unit length between the two phases. Finally* ***r*** *is the series resistance of the transmission line per unit length.*

In Fig 2 the input to the horizontal shift register is in the plane denoted with x=0 and the end of the horizontal register denoted with x=L is inside the imager and not available for measurement. U1 and U2 are the voltages applied to the imager pins for the quasi 2-phase transport and I1 and I2 are the related currents. Only the first and the last section are drawn. The resistance per unit length is r; C is the coupling capacitance per unit of length between the gates and C0 the capacitance per unit length with respect to ground. Through the transformation of variables I=I1-I2; U=U1-U2 and In=I1+i2; Un=U1+U2 and making use of symmetry properties of the design the equations are uncoupled and hence simple to solve.
The unknown transfer function, that determines the distribution of the clock signal over the CCD, is governed by the following 2 differential equations (the other 2 for Un and In are only needed for the input impedance):

$$\frac{d}{dx}I(x,t) := (C0 + 2\cdot C)\cdot\frac{d}{dt}U(x,t)$$

and

$$\frac{d}{dx}U(x,t) := r\cdot I(x,t)$$

Which, after additional differentiation and substitutions, leads to a set of two second-order differential equations:

$$\frac{d}{dx}\frac{d}{dx}I(x,t) := (C0 + 2\cdot C)\cdot r\cdot\frac{d}{dt}I(x,t)$$

$$\frac{d}{dx}\frac{d}{dx}U(x,t) := (C0 + 2\cdot C)\cdot r\cdot\frac{d}{dt}U(x,t)$$

with boundary conditions

$$\frac{d}{dx}U(L,t) := 0$$

$$U(0,t) := V$$

The transfer function with the worst-case condition for the clock distribution over the horizontal registers is given by:

$$H(f) := \frac{U(L,f)}{U(0,f)}$$

After solving the DV and substitution the result obtained is:

$$H(f) := e^{-\lambda(f)\cdot L}\cdot\left(1 + \tanh\left(\lambda(f)\cdot L\right)\right)$$

Since the transfer function H(f) is a non-observable function the behavior must be estimated in another way. For this purpose the input impedance is derived as:

$$Z(f) := \frac{2 \cdot r}{\lambda(f) \cdot \tanh(\lambda(f) \cdot L) + \mu(f) \cdot \tanh(\mu(f) \cdot L)}$$

With parameters

$$\lambda(f) := \sqrt{1j \cdot 2 \cdot \pi \cdot f \cdot r \cdot (C0 + 2 \cdot C)}$$

$$\mu(f) := \sqrt{1j \cdot 2 \cdot \pi \cdot f \cdot r \cdot C0}$$

This input impedance (In Fig 4 denoted as S11) contains the same parameters as the transfer function and is measurable. Based on these measurements an estimation could be given for the performance of the imager in 2-speed operation.
The measurements and the derived models relate to the distribution of the clock signals for the image-array, the storage-array and the horizontal shift register.

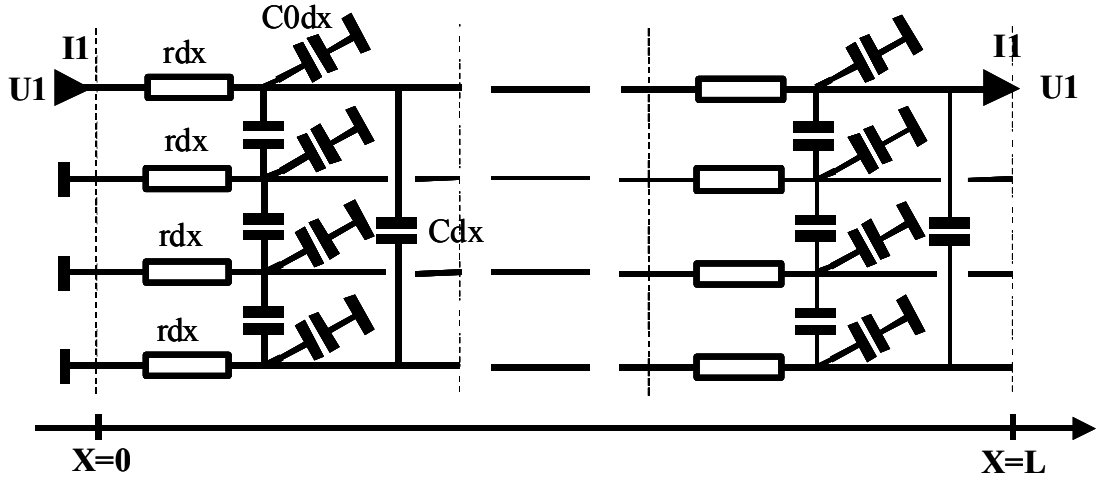

Fig3: *Electrical replacement diagram for the vertical clock distribution. This model holds for the distribution of the clock signals for both image and storage array.*

Determining the transmission line parameters
Using a network analyzer with a reflectometer setup one can measure the equivalent series resistance and series capacitance of the two-ports. The latter are the inputs to the imager and hence the input for the bus bar that distributes the clock.
In the upper part of Fig 4 the measurement of the input impedance for the Image and Storage clocks are given in a Smith-Chart. The horizontal axis shows the real part of the impedance and the vertical axis the imaginary part. The impedance crosses the real axis at some point showing that there is also some self-inductance in the circuit. The marker is put at 9.48MHz, which is close to the 2-speed fast vertical transport frequency. The series R and C at that frequency are: 17 Ohm and 916 pF for the image clock and 7.2 Ohm and 1.66nF for the storage clock.
The lower part of Fig 4 is depicting the input impedance of the horizontal clocks when driven in quasi 2-phase. The frequency sweeps from 1 MHz to 200 MHz. At 74 MHz, near the driving frequency in 2-speed mode, the equivalent series resistance is 24 Ohm and capacitance is 88 pF.

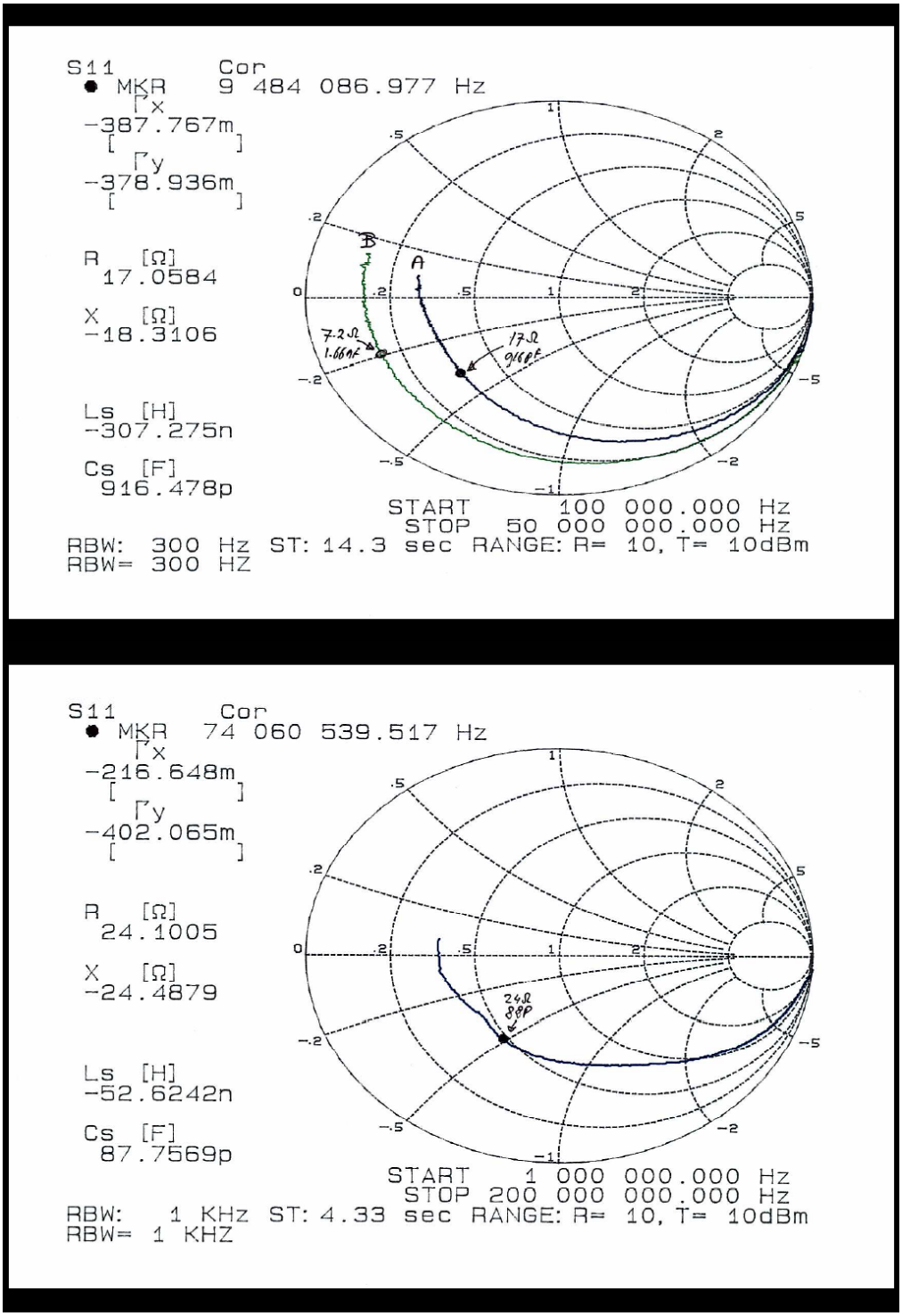

Fig 4 : *Smith-chart plots of the input impedance for image and storage clocks (upper graph) and horizontal clocks (lower graph) in quasi 2-phase usage. The plots show at the marker frequency the equivalent series resistance and capacitance.*

A prior condition for the transmission line approach to be applicable is that the clock-bus-bar must be designed in low-skew fashion. Remembering that the transport of a charge packet in a CCD is driven by the voltage difference between the consecutive phases of the clocks. In a low skew design the driving voltages generated in the silicon for transporting the charge packets are mainly determined by the distribution of the clocks in the imager, e.g. the bus bar.

Graceful degradation of charge transport.
One of the major advantaged of dealing with charge transport in CCD imagers it's the fact that using it above the 3dB-frequency only shows up as a reduction of the maximum charge packet that can be transported [12] and in transport efficiency. This could be called a graceful degradation of charge transport. A parameter that is allowed to have degradation without having any effect on image quality since it can be handled very well.

For 2-speed operation the vertical transport is done at an effective speed of 9.3 MHz and reading the horizontal shift register is at 2x74MHz resulting in a net pixel rate of 148Mpps. As an example: application of special circuitry enhanced the horizontal clock distribution, green trace in right part of Fig 5.

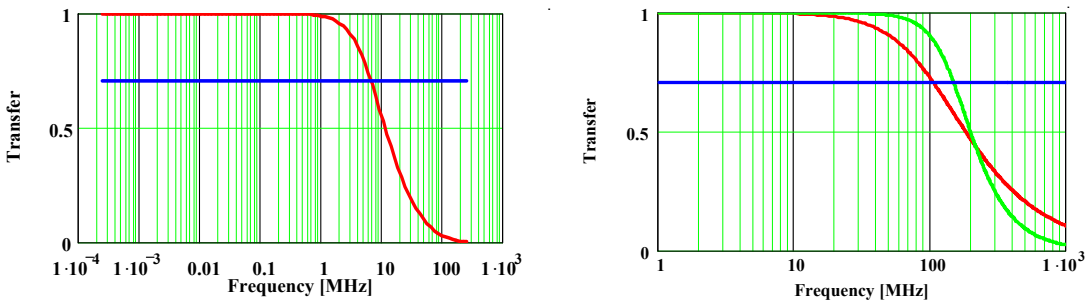

Fig 5: *Clock signal distribution. Shown is the ratio between the voltage swing at the end of the transmission line and the driving voltages at the input; transfer function. It's that point for the clock distribution with maximum attenuation. For purpose of reference the -3dB point is also given***.**

The performance is even better than depicted in Fig 5 due to the fact that the driving voltages are near square-wave shaped and the amplitude of the fundamental frequency is $4/\pi$ times the square wave amplitude. A fact often used by manufactures in defining the MTF, the square wave MTF is always better! Hence the clock is allowed to decrease almost 3 dB before a noticeable effect will occur.

The right part of Fig 5 shows the transfer function for the horizontal register during quasi 2-phase charge transport. It is for the worst-case point at the horizontal register bus bar. The 3dB point is at about 100 MHz (red curve) and with special circuitry at 150 MHz (green curve).
In the left part of Fig 5 the estimated transfer function for the storage clock is given. Without special circuitry it's 3 dB point runs up to about 7 MHz.
In both graphs the blue line denotes 3dB attenuation.

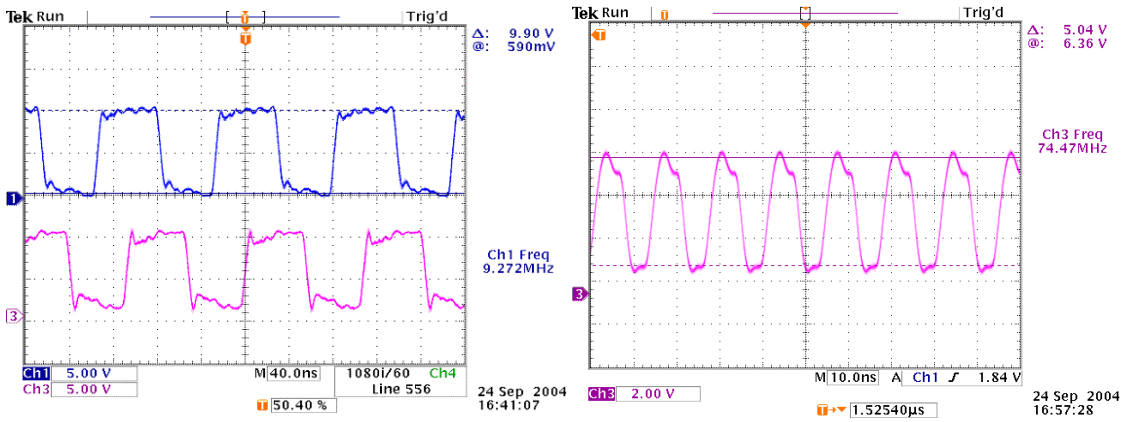

Fig 6*: The generated clock for fast vertical transport during 2-speed imager/camera operation is shown in the left part of figure 6. These pulses drive the image and storage array of the imager during the vertical blanking. In that time the charge image is transport into the storage array. These clocks are measured while driving the 3 imagers in parallel. The upper trace shows the clocks to the image array and the lower trace to the storage array. The right part of figure 6 shows the horizontal clocks.*

4.0 CONCLUSION

Based on the HD-DPM imager a camera platform was conceived that enables the design of a switchable single speed and double speed HDTV camera.

To speedup the design of the 2-speed HDTV camera a mathematical model was derived, based on transmission line theory, for calculating the internal clock distribution for the imager. The internal clock distribution could not be measured but the impedance could. Through the measurement of the input impedance, using Smith-Chart techniques, the parameters determining the clock distribution was extracted. It was shown that the imager was capable of capturing images at 1080i120 and 1080p60, which internally even extended into 1080p120.

The choice for 2 horizontal shift register and outputs, instead of the more common 1 horizontal shift register and output, enables many advantages among which a fast track to the 2-speed HDTV camera.

It is the first HDTV slo-motion systems camera that can also be used as a normal state of the art HDTV camera.

The first multi-format and multi-speed HDTV cameras where successfully employed during the June 2004 European Soccer Games in Portugal and the August 2004 Olympics in Greece.

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